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**AMENDMENTS TO THE CLAIMS**

Claims 25-32 and 34-50 remain in the application. By this listing, claims 25, 26, 29-31, 34, 36, and 38-42 have been amended. This listing of claims replaces all prior versions of claim listings in the present application.

**Complete listing of claims.**

Please amend the claims as follows:

1-24. (Cancelled).

25 (Currently Amended). A semiconductor layer arrangement, comprising:

a substrate;

a layer being arranged on the substrate, the layer including a first subregion and a second subregion arranged proximate to the first subregion, the first subregion being a decomposable material and the second subregion having a structure of non-decomposable material;

a covering layer positioned on the layer including the first subregion and second subregion; and

an electrically conductive passivation layer positioned between adjacent surfaces of the non-decomposable material and the covering layer;

wherein the decomposable material is diffusible through the covering layer and the covering layer closes the first subregion off to all area outside the semiconductor layer

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arrangement while the first subregion being mechanically closed off with respect to the outside world.

26 (Currently Amended). The semiconductor layer arrangement according to Claim 24 25, further comprising an intermediate layer between the substrate and the layer of decomposable material and the useful structure.

27 (Previously Presented). The semiconductor layer arrangement according to claim 26, wherein the covering layer and the intermediate layer comprises dielectric material.

28 (Previously Presented). The semiconductor layer arrangement according to claim 26, wherein the covering layer and the intermediate layer comprises any one of silicon oxide, silicon nitride, SiLK, porous SiLK, oxazole, porous oxazole, Black Diamond, Coral, Nanoglass, JSR LKD, polybenzoxazole, polybenzimidazole, polyimide, polyquinoline, polyquinoxaline, polyarylene, and polyarylene ether, and combinations thereof.

29 (Currently Amended). The semiconductor layer arrangement according to claim 24 25, wherein the substrate comprises silicon.

30 (Currently Amended). The semiconductor layer arrangement of Claim 24 25, wherein the covering layer is permeable to decomposable material having decomposed.

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31 (Currently Amended). The semiconductor layer arrangement of Claim ~~24~~ 25, wherein the structure of non-decomposable material is an electrically conductive material.

32 (Previously Presented). The semiconductor layer arrangement as claimed in Claim 31, wherein the structure of non-decomposable material comprises any one of silver, a silver alloy, tungsten, tungsten silicide, aluminum, an aluminum alloy, copper; and copper alloy.

33 (Not Entered).

34 (Currently Amended). The semiconductor layer arrangement of Claim ~~24~~ 25, wherein the structure of non-decomposable material is a dielectric material.

35 (Previously Presented). The semiconductor layer arrangement of Claim 34, wherein the structure of non-decomposable material comprises any one of silicon dioxide, silicon nitride, ceramic material, and combinations thereof.

36 (Currently Amended). The semiconductor layer arrangement of Claim ~~24~~ 25, wherein the decomposable material is thermally decomposable.

37 (Previously Presented). The semiconductor layer arrangement of Claim 36, wherein the decomposable material comprises any one of polyester, polyether, polyethylene glycol, polypropylene glycol, polyethylene oxide, polypropylene oxide, polyacrylate,

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polymethacrylate, polyacetal, polyketal, polycarbonate, polyurethane, polyether ketone, cycloaliphatic polymer, polynorbornene, aliphatic polyamide, Novolak, polyvinylphenol, an epoxy compound, copolymer of these compounds, terpolymer and combinations thereof.

38 (Currently Amended). The semiconductor layer arrangement of Claim ~~24~~ 25, wherein the decomposable material is photosensitive.

39 (Currently Amended). The semiconductor layer arrangement of Claim ~~24~~ 25, wherein at least one support structure is formed in the layer arranged between the substrate and the covering layer.

40 (Currently Amended). The semiconductor layer arrangement of Claim ~~24~~ 25, comprising a protective structure running along a lateral boundary of the substrate.

41 (Currently Amended). The semiconductor layer arrangement of Claim ~~24~~ 25, comprising a passivation layer at least partially surrounding the structure.

42 (Currently Amended). A process for forming a layer arrangement, comprising:

forming a layer on a substrate, the layer including a first subregion and a second subregion arranged proximate to the first subregion, the first subregion having decomposable material and the second subregion having a structure of a non-decomposable material;

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forming a covering layer on the layer including the first subregion and second subregion;  
and

forming an electrically conductive passivation layer at least between ~~adjacent surfaces of~~  
the useful structure and the covering layer;

wherein the decomposable material is removable from the layer arrangement by diffusing  
through the covering layer ~~resulting in a layer arrangement in which~~ while the first  
subregion is mechanically closed off to all area outside the layer arrangement.

43 (Previously Presented). The process of Claim 42, further comprising causing the  
decomposable material to be removed from the layer arrangement.

44 (Previously Presented). The process of Claim 43, where the decomposable material is  
caused to be removed from the layer arrangement by thermal decomposition.

45 (Previously Presented). The Process of Claim 42, wherein the structure is formed  
from copper and is at least partially sheathed by a passivation layer being formed from  
any one of cobalt-tungsten-phosphorus, cobalt-tungsten-boron, cobalt-phosphorus or  
ruthenium and combinations thereof by means of an electroless deposition process.

46 (Previously Presented). The Process of Claim 42, wherein the structure is formed  
from copper and is at least partially sheathed by a passivation layer being formed from  
any one of tantalum, tantalum nitride, titanium nitride, tungsten, tungsten nitride or

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tungsten carbide and combinations thereof by means of a chemical vapour deposition process.

47 (Previously Presented). The Process of Claim 42, wherein forming a layer on the substrate further comprises:

depositing and patterning the decomposable material on the substrate; depositing the material of the structure on the substrate; and planarizing the surface of the deposited decomposable material and material of the structure.

48 (Previously Presented). The process of Claim 42, wherein forming the layer on the substrate further comprises:

depositing and patterning material of the structure on the substrate;

depositing the decomposable material on the substrate; and

planarizing the surface of the deposited decomposable material and material of the structure.

49 (Previously Presented). The process of Claim 42, further comprising forming at least one additional layer stack on the covering layer, the additional layer stack having an additional covering layer on an additional layer comprising decomposable material and a useful structure.

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50 (Previously Presented). The process of Claim 49, wherein structures that are separated by a covering layer are coupled by at least one contact hole being introduced into the covering layer and being filled with electrically conductive material.